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Low Power PLL for Communication System

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ABSTRACT

This paper presents the design aspects of low power digital PLL. The performance determining parameters of a digital PLL are lock range, capture range, jitter in generated output signal and power consumption. Its performance is mainly governed by two building blocks namely the voltage controlled oscillator (VCO) and phase detector. We have performed the complete analysis of phase noise and power consumption of current starved VCO, a novel D flip-flop based phase detector and transmission gate based charge pump. We have introduced a charge pump which is giving a remarkable reduction in reference spur. As PLL is used for many applications like as a frequency synthesizer, for clock deskewing, for jitter reduction, in FM radios so everyone demands a low cost low power highly integrated PLL design. Best efforts have been made to design a MOSFET based low power, low cost GHz range digital PLL. The main objective of this paper is to design a low power digital PLL which produces a very stable clock signal having jitter less than 1ps,power consumption less than 805uw ,output frequency ranged from 0 to380MHz at a supply voltage of 1.8V.

Keywords**:** phase frequency detector (PFD), phase locked loop (PLL), charge-pump (CP), True single phase clock (TSPC), low - power, low-jitters

1. INTRODUCTION

PLL is a very important block in almost every communication system. It is a tracking communication block in which output frequency is either equal to reference frequency or it is

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integral multiple of input reference frequency in case when divider is used in feedback path. PLL has number of applications like performing phase modulation/demodulation, in FM radios, in transceiver design, for jitter and noise reduction, in frequency synthesis to generate new frequencies which are integral multiple of a single stable frequency which is conventionally generated by a crystal oscillator and its peculiar advantage is that the generated frequencies have the same stability as the reference frequency.

PLL technique for frequency synthesis is in practice from 1930's but that time it required a huge implementation cost. Now-a-days, we require to design a PLL having higher capture and lock ranges, lower design cost, low power consumption, low jitter and low noise.

In this paper the detailed and accurate analysis of PLL is carried out having a precharge type phase detector, transmission gates based charge pump, ring oscillator based VCO and second order loop filter. The circuit is simulated using CADENCE design tool.

2. LITERATURE REVIEW

High speed and low power phase frequency detector (PFD) designed with modified TSPC using 19 transistors is given in [1]. A MEMS phase detector at X band based on MMIC technology and composed of a power integrator, power sensor is given in [2]. High voltage diode based charge pump using .35 μm technology is given in. Interpolated VCO design for low bandwidth, low jitter using 45nm technology is given in [3-5].

3. THE PROPOSED PLL ARCHITECTURE

The basic PLL architecture is given in figure 1. It consists a phase detector that compares the phase difference between the input reference signal and the VCO output, a low pass filter which removes high frequency component from error signal and a VCO whose output frequency is controlled by the input error signal.

In our proposed PLL architecture we have used MOSFETs to design every block so that the power consumption is reduced considerably.

The proposed design consists the following blocks:

1) Phase frequency detector with recharge technique (PFD).
2) Transmission gate based charge pump.
3) 15 inverter stages current starved VCO.
4) Programmable divider.
5) Second order loop filter.

The above building blocks used in PLL circuit under lock condition gives a stable output signal. The magnitude response of low pass filter determines the capture range of designed PLL and the output of VCO given as negative feedback to phase detector determines the Lock range. Using divider in feedback path we can generate integral multiple frequencies of single reference frequency at output [6-13].

Inverter stage based VCO

VCO is an electronic circuit in which output frequency is controlled by input voltage. Conventionally varactor diode exhibits voltage variable capacitance which in turn leads to dependency of output frequency on input voltage, but to get the higher output frequency range with input controlling voltage at a high degree of stability, low noise and low power consumption we are using 15 inverter stages ring oscillator based VCO

We know the time period of generated square wave by ring oscillator is $2*N*T_{pd}$ where T_{pd} is propagation delay of each stage and N be the number of inverters in ring. So output frequency of generated wave is given by

$$f_{out} = \frac{1}{2NTpd}$$

So to design a VCO this T_{pd} of each stage should vary with input voltage. The propagation delay T_{pd} of a single inverter is controlled by the voltage applied on that inverter. In our proposed design this is achieved by using current starved technique. VCO design is given in Figure 1.

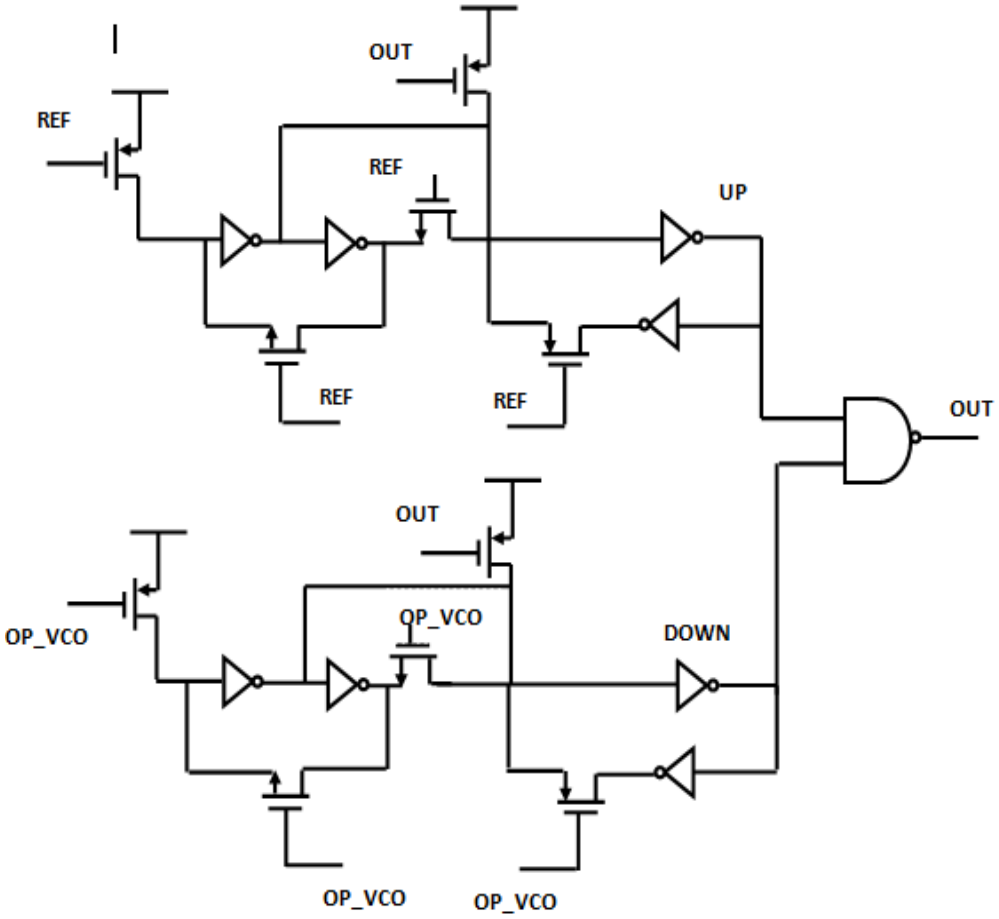

Figure 1. Phase frequency detector

In our design we have used current starved controlling MOSFETS in alternate stages to get a proper swing of output voltage. NM1 is controlling NMOS its drain consists of cascade series of current starved PMOS and its source has cascade series of NMOS.

When input to NM1 is less than its threshold voltages it will be in cut-off as a result its drain will be at V_{dd} and source will be at ground due to this corresponding gate voltage of cascaded controlling MOSFETS will make them to offer high resistance in their respective stage due to which T_{pd} of all stages will be high and generated output frequency will be low. When input to NM1 is increased its resistance will decrease and a current will flow from V_{dd} to ground due to which the drain and source terminal voltage of NM1 will decrease and increase respectively due to which resistance of each starved MOSFETS will decreased and as a result the propagation delay of all stages will reduced and output frequency will increase correspondingly. So in this way we get a variable output frequency as a function of input control voltage.

Precharge phase detector

Conventionally phase difference between any two sinusoidal signals can be found by using multiplier followed by a low pass filter but the phase detection range by this is very low with less accuracy. In our proposed design we have used two D-flip flops with a reset circuit to get accurate phase difference between two signals in terms of width modulated pulses [14-18].

Charge pump

Charge pump is an electronic circuit which generates a controlling voltage proportional to width modulated pulses of precharge phase detector. This is a very important block in PLL architecture. Phase detector produces width modulated pulses corresponding to phase difference between reference and VCO_{out}, and corresponds to these modulated pulses charge pump generates a controlling voltage.

We have designed a transmission gate based charge pump. In the proposed architecture we have used 2 current sources , transmission gates which switches according to UP and Down signal given by phase detector and a output capacitor C. The proposed design is given in Figure 2

- When UP = 1 and DOWN = 0 ($VCO_{out}$is lagging behind ref.) then a charging current will flow into the capacitor C as given by current source I_1 through tramission gate $T_1$and output voltage will increase which in turn makes VCO to oscillate at greater frequency.
- UP = 0 and DOWN = 1 (VCO_{out} is leading ref.) then a discharging current flows from C to ground as I_2 through gate T_2 and output capacitor voltage will decrease correspondingly and so as VCO frequency

Transmission gates T3 and T4 provides a discharging path to current sources I1 and I2 When T1 and T2 are in off state respectively.

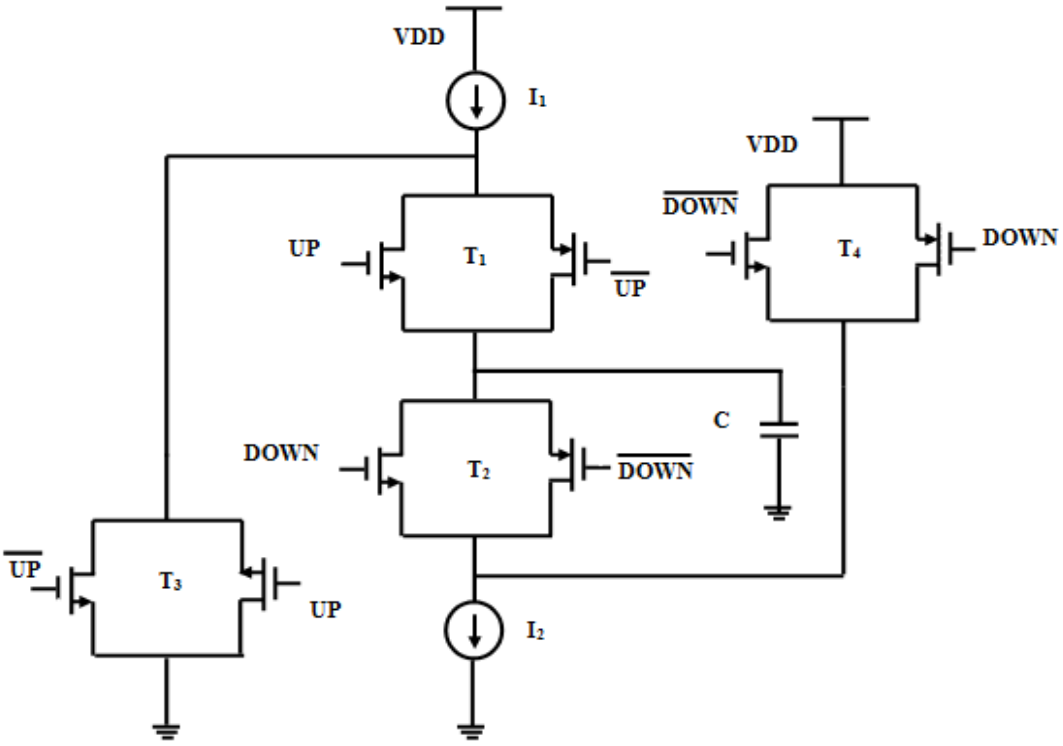

Figure 2. Charge pump

Loop filter

Loop filter is basically a low pass filter which removes the high frequency components from charge pump output. The magnitude response of loop filter determines the capture range of PLL. Second order filter is being used in our design consists Of a series R-C branch in parallel to C. We know cut off frequency of passive filter is determined by the values of passive components used like resistors and capacitors.

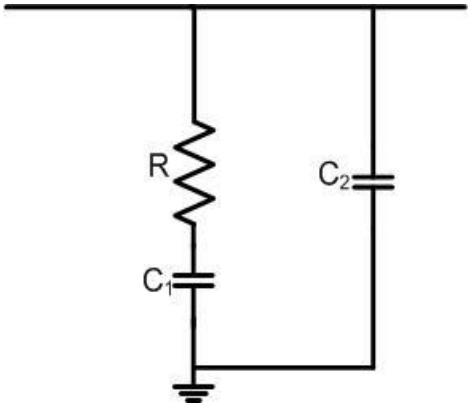

Figure 3. Loop Filter

4. SIMULATION AND RESULTS

We have designed and simulated all the building blocks required to design a PLL using gpdk180 library of CADENCE analog environment. The output follows the reference signal in 13.5 usec which is shown in Figure 4. In our proposed design maximum frequency which can be tracked is 380 Mhz. Using our design obtained jitter is less than 0.9 psec as we can see in eye diagram which is given in fig. 6. The average power consumption of our circuit is 802 uW. All the obtained parameters are tabulated in Table 1.

To obtain precise frequency tracking we have used 15 inverters in ring of starved voltage controlled oscillator (VCO). Low pass filter is designed with RC values as R1 = 10 kΩ, C1 = 200 pf, C2 = 100 pf.

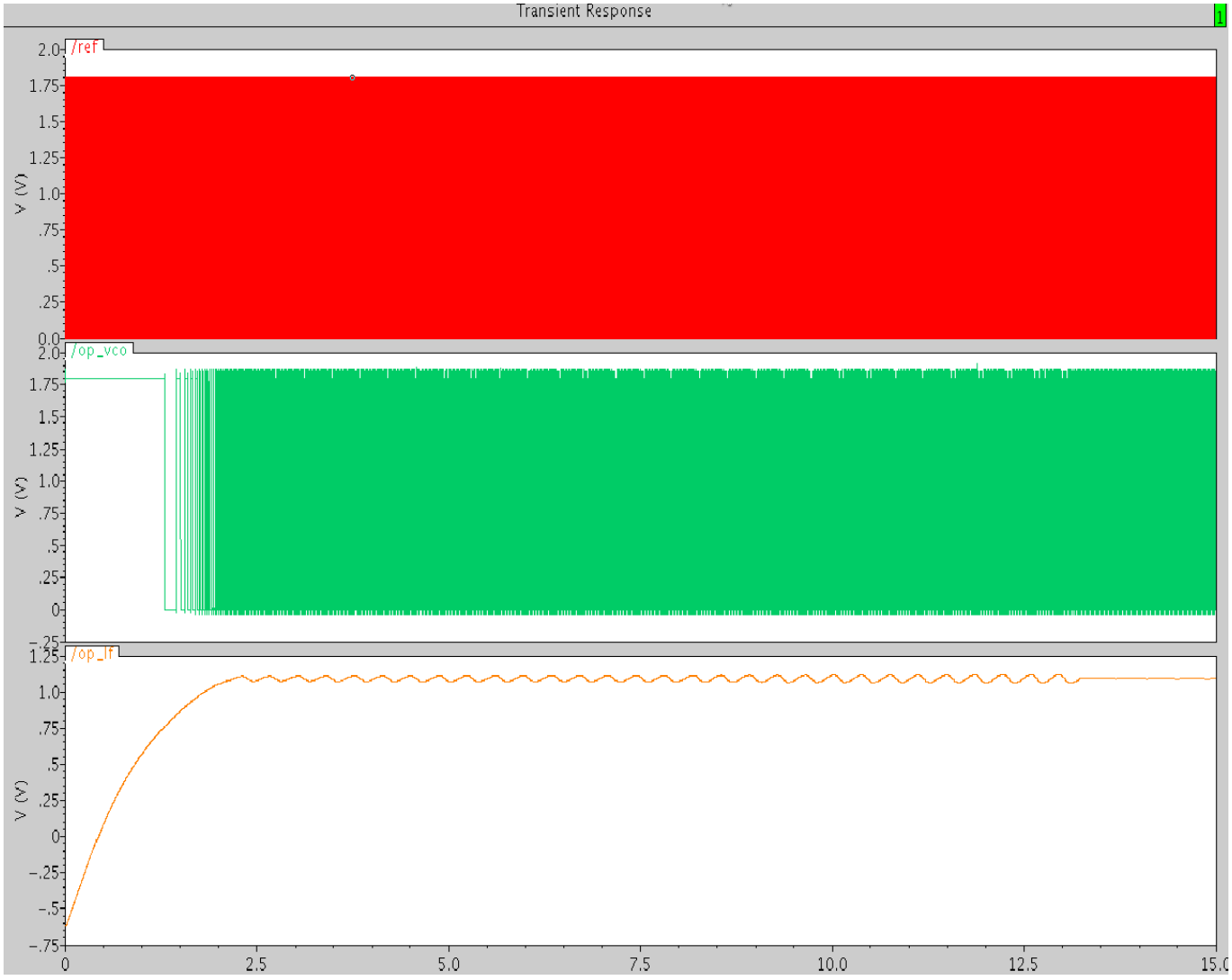

Figure 4. Output of PLL

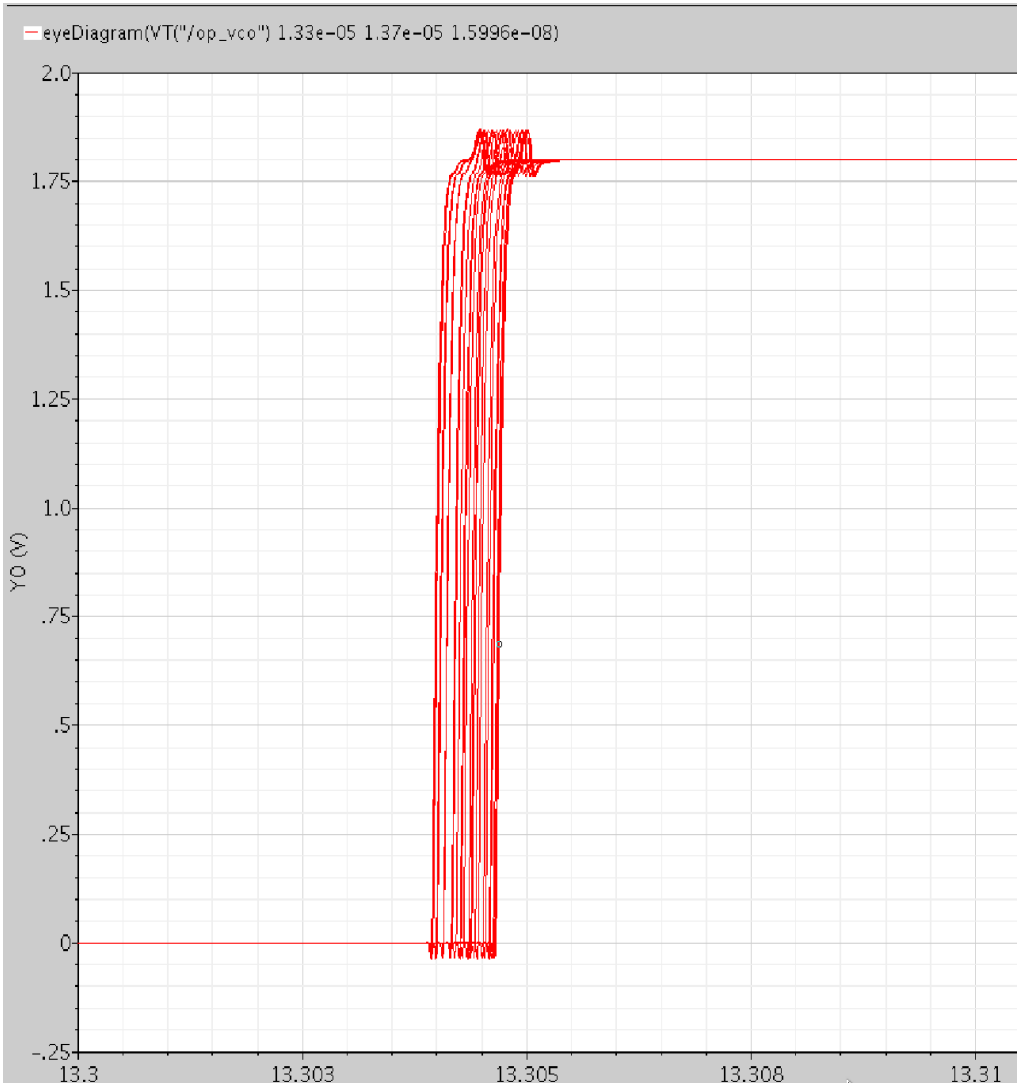

Figure 5. Eye Diagram for calculation of jitter

Table 1. Output results

Parameter	Value
VDD	1.8 Volts
Technology	GPDK180 nm
Average Power	802 uW
Jitter	0.9 psec
Frequency Range	380 Mhz

5. CONCLUSIONS

Using proposed design the power consumption of digital PLL is reduced to less than 802 uW at a supply voltage of 1.8V.The maximum frequency which can be tracked by our design is 380M Hz. The jitter is reduced to less than 1ps. We have designed the phase detector using MOSFET based D flip-flop and charge pump is designed using transmission gates so by using all new digital blocks in our PLL we have reduced power to such an extent. The output swing range of VCO is increased using controlling starved MOSFETS in alternate stages inspite of using in all stages. By embedding some new digital techniques we are further working on its design to get a better output frequency range and jitter much lesser than what we got.

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