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Barrier modification of Al/PS/c-Si Schottky contact based on porous silicon interfacial layer

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ABSTRACT

This paper presents the fabrication and characterization of the different types of porous silicon PS (n-type and p-type) were used as a semiconductor to modifying Schottky contacts (Al/p-PS, Al/n-PS) and ohmic contact (Al/p-Si, Al/n-Si) respectively. Porous layer formed by electrochemical and photo-electrochemical etching. Barrier height, ideal factor, series resistance, are carefully figured out and compared with (I-V, C-V) measurements, H(I) and F(V) equations. The ideally factor was very high and the value of the Schottky barrier height of p-type sample was larger than that of n-type for all methods were use in this study. Also, higher series resistance for Al/PS/p-Si Schottky diode as compared to Al/PS/n-Si Schottky diode while the junction exhibits strong rectifying characteristics for n-type as compared of p-type.

***Keyword*:** Porous silicon, Schottky barrier height, electrochemical etching, Norde method

1. INTRODUCTION

Due to the technological importance of metal-semiconductor Schottky contacts, a full understanding of their current–voltage (I–V) and capacitance–voltage (C–V) characteristics are of great interest [1].The junctions between a metal and a semiconductor find numerous applications in microelectronic devices and porous silicon PS is a very promising material due

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to its excellent properties and compatibility with silicon based microelectronics with reduced fabrication cost [2]. Porous silicon PS has unique properties such as direct and wide modulated energy band gap, high resistivity, vast surface area-to-volume ratio and the same single-crystal structure as bulk Si [3]. Porous silicon structures are produced by electrochemical etching of silicon wafers in organic solutions of acetonitrile (CH_3CN) or dimethyl-form-amide (C_3H_7NO) containing hydrofluoric acid (HF) [4]. Typically, the PS layer is sandwiched between the c-Si substrate and a metallic contact. Interfaces between metals and semiconductors are complex regions whose physical properties strongly depend on the preparation conditions of the surface and [5].

The interface states and chemical reactions between metals and semiconductors at the interface play an important role in the electrical properties of devices [6]. There are a number of factors that can produce barrier inhomogeneity such as non-uniformity of the interfacial charges [7]. Differently from a p-n junction, the current transport in a metal/semiconductor junction is mainly due to majority carriers, that is to electrons for n-type or holes for p-type semiconductors. The emission of thermally excited electrons (or holes) from the semiconductor to the metal over the potential barrier (thermionic emission, TE) is the dominating process contributing to the metal/semiconductor junction current [8].

Other mechanisms that may contribute to the metal/semiconductor current are generation/recombination in the space-charge region, diffusion of electrons in the depletion region or injection of holes from the metal that diffuse in the semiconductor and recombine in the neutral region. In addition, there may be edge leakage current due to high electric field at the metal-contact periphery or interface current due to traps at the metal/semiconductor interface [8-10]. Ohmic contacts are generally formed using heavily doped Schottky contact so as to reduce the initial barrier. The barrier height of a Schottky diode is carried out in more than one method: such as current-voltage (I-V) characteristics and capacitance-voltage (C-V) measurement.

We demonstrate the rectifying behaviour of the Schottky diode on both Al/PS/p-Si and Al/PS/n-Si. In this paper, effect porous silicon layer type as interface contact Schottky barrier height was presented. This paper presents results to the effect that type of porous silicon layer as interface Schottky barrier height with

2. MATERIALS AND METHODS

The porous silicon layers were produced by electrochemical etching ECE and photo-electrochemical etching PECE on one side mirror p-type ($N_A = 2.75 \times 10^{14}\ cm^{-3}$) and n-type ($N_D = 8.35 \times 10^{14}\ cm^{-3}$) wafer silicon (111) orientation. The substrate material p and n-type silicon have the same value of resistivity($16\ \Omega \cdot cm$).mixture of 40 % HF: 99.9 % Methanol (50:50) was used to etching in dark for p-type and subjected to external illumination with a 40 mW diode laser 650 nm for n-type. Duration etching time and current density were 12 min and 24 mA/cm^2. In the previous reported Hadi *et al*, used the simplest cell as Schematic diagram of electrochemical anodization system was reported [11]. The process formed by the following steps:

- Coated thick layer of aluminum on the backside of wafer silicon.
- The Si wafer samples was cuts to 1×1 cm^2.

- Cleaning of <111> p- and n-type Si wafer by immersing in the Methanol and alcohol turn in the ultrasonic bath for few minutes.
- Rinsed in distilled water treated ultrasonically
- Drying in a hot air stream.
- ECE technique for PS layer in p-type wafer
- PECE technique for PS layer n-type wafer
- Oxidation (400℃, 30min) porous silicon layer

And Ohmic contacts on both PS (semi-transparence- nanometer thick) and bulk silicon (μm thick-back side) were made by deposition of high purity Al films by using thermal resistive technique under vacuum pressure of 10^{-6} torr, using an evaporation plant model "E306 A manufactured by Edwards high vacuum". After evaporation process, thickness of evaporated film on a glass substrate was measured using gravimetric method. In gravimetric method, "Mettler AE-160 digital with accuracy of 10^{-4} gm" is used to weight the samples. The IV tracing for the porous silicon – Aluminum junction was conducted with the help of a using UNI-T UT61E Digital Multimeters and dc. Power supply type LONG WEI DC PS-305D 30. The capacitance–voltage CV measurements were performed by using hp4275AmuTi-frequaency LCR meter–HEWLETT Packard (MHz) at room temperature.

A sectional view of the Schottky junction Al/PS/n-Si/Al and Al/PS/p-Si/Al are shown in Fig. 1, metal semiconductor metal hetero-structures. In this experiment, we fabricated Schottky barrier MOS for N and P-type (for electron and hole transportation) and Compare between barrier height calculated from Al/PS/n-Si/Al and Al/PS/p-Si/Al devices by four methods: Current –voltage measurement, Capacitance-voltage measurement, Norde and H(I) function[12].

3. RESULTS AND DISCUSSION

Figure 1 presents the cross-sectional view and the room temperature experimental forward and reverse bias dark IV characteristics of Al/PS/n-Si/Al and Al/PS/p-Si/Al Schottky barrier. Referring to the dark IV curve of Fig. 1, it was shown two regions; the first one recombination center region at low voltage and tunneling region in the interface junction at high voltage. The thermionic emission theory assumes that electrons, with energy larger than the top of the barrier, will cross the barrier provided they move towards the barrier. The actual shape of the barrier is hereby ignored. The current can be expressed as Eq. (1) [12]:

$$I = A^{*}T^{2}e^{-\frac{q\,\emptyset_b}{KT}}\left(e^{-\frac{qV}{KT}}-1\right) \quad \text{..... (1)}$$

where: A^{*} is the Richardson constant and $\emptyset_b$ is the schottky barrier height. Majority carriers are able to cross the potential barrier much easier than at low voltage bias results in reducing the height of the potential barrier, so that the diffusion current becomes greater than the drift current. The roughness of the PS surface and an in-homogeneously structure leads to get high ideal factor. Also, recombination of electrons and holes in the depletion region and the increase of the diffusion current due to increasing the applied voltage [13].

The rectification factor is evident that the junction exhibits strong rectifying characteristics. It is determined as of 10^3 for Al/PS/n-Si and 10 for Al/PS/p-Si at ±2 V.

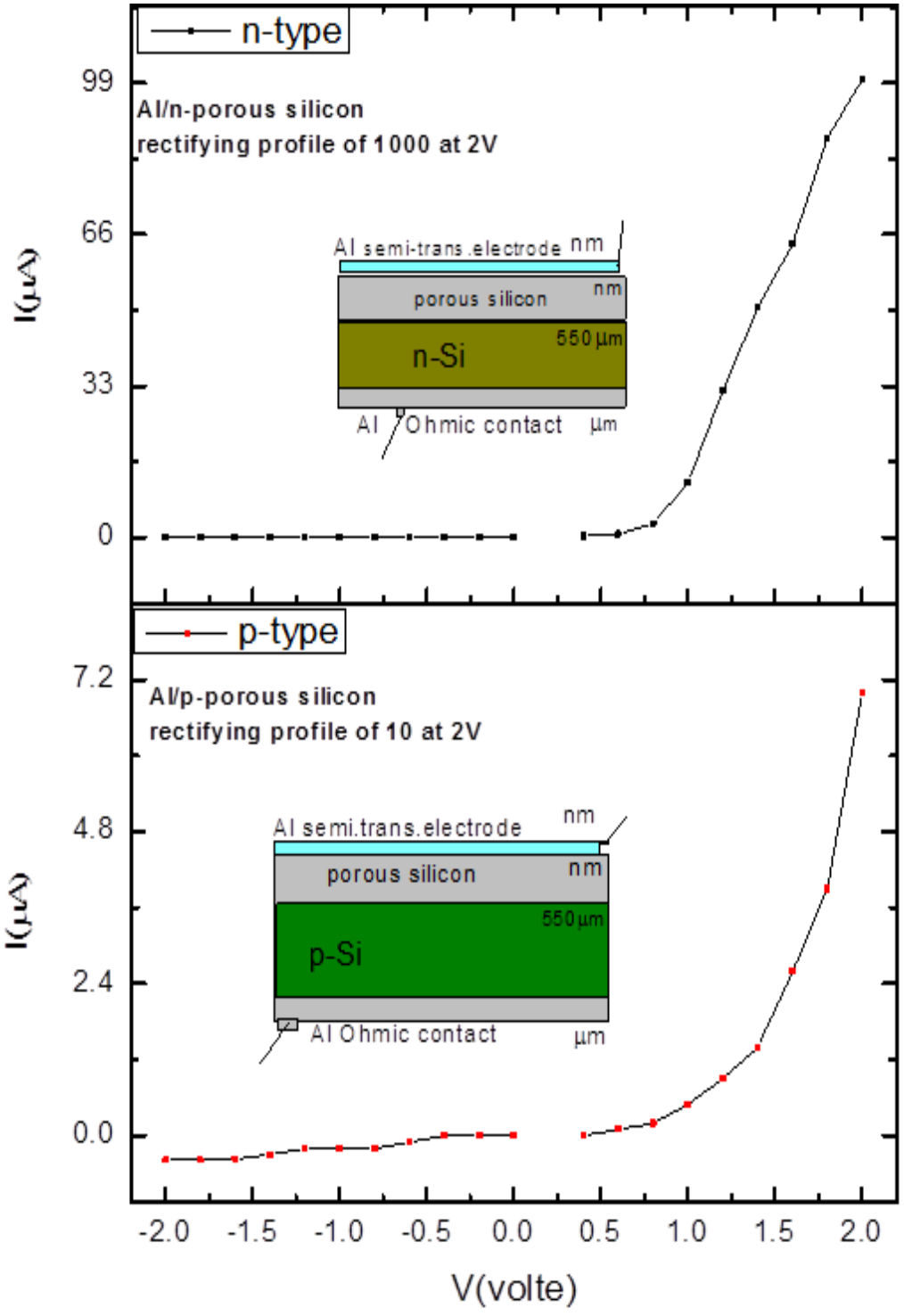

Figure 1. The plot of the forward and reverse bias IV characteristics and the cross-sectional view for Al/PS/n-Si/Al and Al/PS/p-Si/Al at room temperature

The barrier height is commonly calculated from the saturation current I_s determined by an extrapolation of log (I) versus V curve. Series resistance is not important in this extrapolation because the saturation current is very low and I_s is strongly depends on the Schottky barrier height, the lower it is the better is the diode. The barrier height $\emptyset_b$ is calculated from I_s in Eq. (2). According to the thermionic emission theory, the diode saturation current is related to the Schottky barrier height by the following equation [12].

$$\emptyset_b = \frac{KT}{q} \ln\left(\frac{AA^*T^2}{I_s}\right) \quad \text{.....(2)}$$

$$n = \frac{q}{KT} \left(\frac{\partial V}{\partial lnI}\right) \quad \text{..... (3)}$$

where: A^* equal 32 and 112 for p-type and n-type silicon respectively the ideal factor, barrier height and the Series resistance for Al/PS/p-Si/Al and Al/PS/n-Si/Al are calculated using equations (1), (2), (3) and $R_S = \partial V/\partial I$ (V = 0). Our results summarized in table1. The ideality factor determined from the slope of the linear region of the forward bias (∂lnI-V) characteristic through the relation in Eq. (3). The ideal factor usually has a value greater than unit for practical diodes. The high ideal factor can be attributed to the sum of the ideal factor of the individual rectifying junctions (i.e., the actual PS/c-Si heterojunction junction and Schottky diodes at the Al/PS or the two metal-semiconductor junctions (Al/PS, c-Si/Al) of a diode ideally have Ohmic characteristics). Schottky junction is not ideal when ideal factor much larger than 2 [14].

Table 1. The barrier height, ideal factor, series resistance and saturation current of Al/PS/p-Si/Al and Al/PS/n-Si/Al Schottky diode from (I-V) characteristics

Silicon type	**p-Si**	**n-Si**
Saturation current I_s	0.0013 μA	0.233 μA
Barrier height $\emptyset_b$	0.91	0.81
Ideal factor n	13	7.9
Series resistance kΩ	750	266

The barrier height can be measured accurately by taking H versus current I as shown in Fig. 4. H-function is defined as [12].

$$H = V - \frac{nKT}{q} \ln\left(\frac{I}{I_s}\right) = IR_s + n\emptyset_b \quad \text{. .....(4)}$$

It will be noticed from the equations for the H-function depend on I-V values and a plot of H versus I has a slope of R_s, also give a straight line with y-axis intercept equal to an $n\emptyset_b$.

Barrier height was obtained by substituting the ideal factor value and the data of the downward curvature region in the forward bias I-V graph from Eq. (4). From H(I) function versus I, the barrier height, shunt resistance and series resistance values were measured and presented in Table 2.

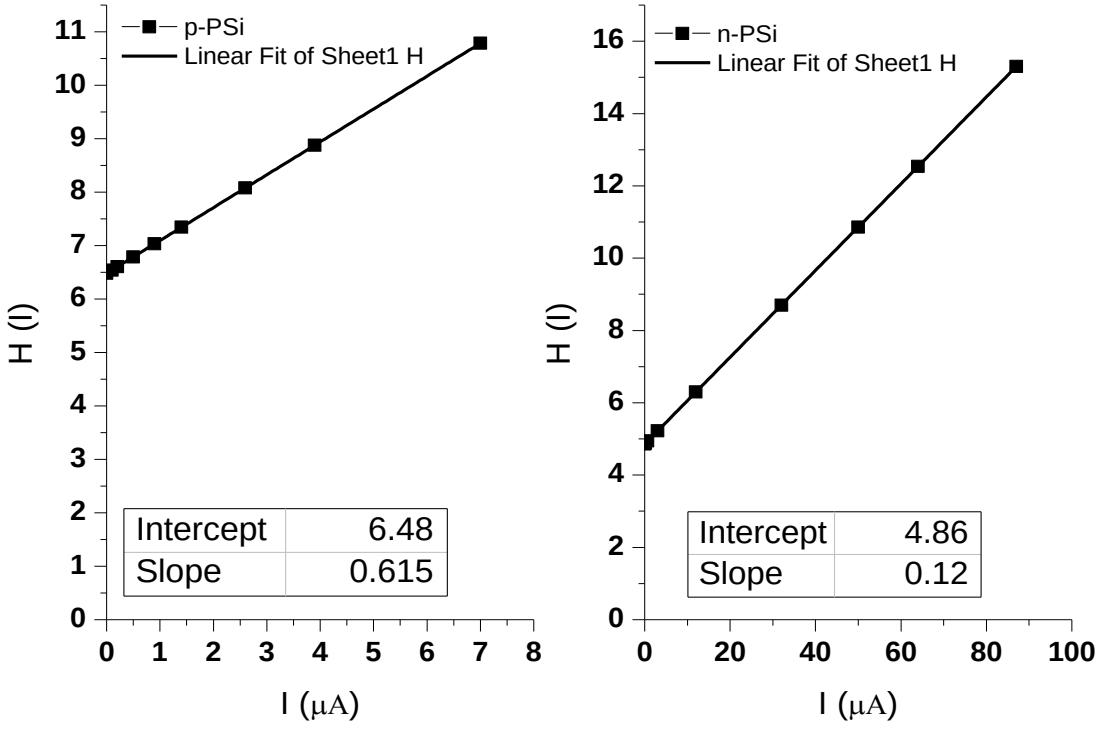

Figure 2. H (I) versus I graphs obtained from forward bias I-V characteristics of Al/PS/n-Si/Al and Al/PS/p-Si/Al Schottky diode.

Table 2. Barrier height, series resistance, shunt resistance and ideal factor of Al/PS/n-Si/Al and Al/PS/p-Si/Al Schottky diode from H (I) function

Wafer silicon	Series resistance $\mathbf{R_s}$ $(\mathbf{k\Omega})$	Shunt resistance $\mathbf{R_{SH}}$ $(\mathbf{M\Omega})$	Intercept $(n\emptyset_b)$	Ideal factor **n**	Barrier height $\emptyset_\mathbf{b}$
p-type	615	3.53	6.48	8	0.81
n-type	120	2.36	4.86	6	0.78

Norde's method is used to evaluate the barrier height of the Schottky contact. A Norde method of measuring the barrier height is describe by plotting F versus V assumes the ideal factor equal one, while as shown in the Fig. 5, the our results was not accuracy because of the large value of ideal factor and the statistical error is increased by using only a few data points near the minimum of the F versus V curve [12], but it was agreement with other result from IV, CV measurements and H(I) function were the barrier height of n-type device large than p-type as shown in Table 3. In this method the minimum F-value $F_{(V_{min})}$, found at V_{min} [12]:

$$F(V) = \frac{V}{2} - \frac{KT}{q}\ln\left(\frac{I}{AA^{*}T^{2}}\right) \quad \text{..... (5)}$$

and barrier height was calculated by the following function has been derived in the modified Norde method [12]:

$$\emptyset_b = F_{(V_{min})} - \left(\frac{1}{2} - \frac{1}{n}\right)V_{min} - \left(\frac{2-n}{n}\right)\left(\frac{KT}{q}\right) \quad \text{.....(6)}$$

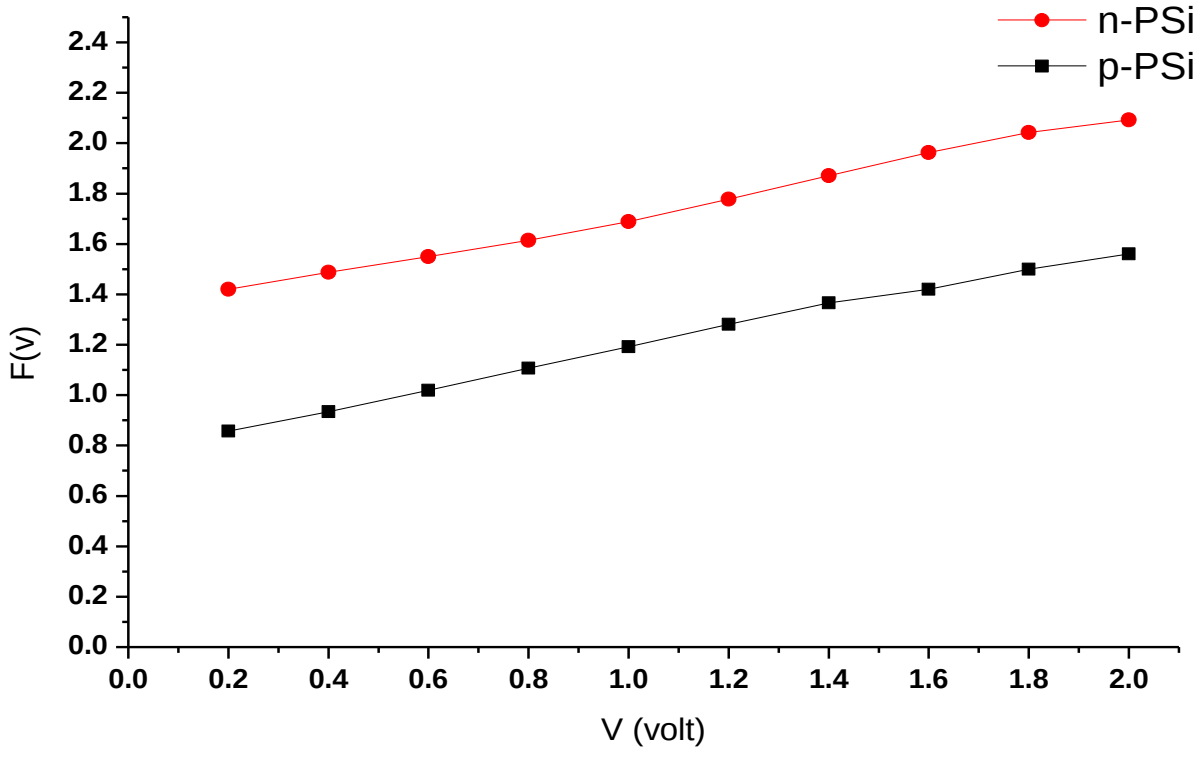

Figure 3. F (V) versus V plot of Al/PS/n-Si/Al and Al/PS/p-Si/Al Schottky diode.

Table 3. Electrical parameters obtained from Norde method Al/PS/n-Si/Al and Al/PS/p-Si/Al Schottky diode.

Wafer silicon	$F_{(V_{min})}$	V_{min}	Ideal factor **n**	Barrier height $\emptyset_b$
p-type	0.77	0.2	8	0.69
n-type	0.57	0.2	6	0.52

Fig. 4. shown The capacitance-voltage and C^2-V of the Al/PS/n-Si were measured at frequency of 200KHz in dark at room temperature, plotting C^2-V, a straight line is obtained, we determine that the barrier height for two devices were the sum of the built-in potential in Schottky contact by using Eq. (7).The capacitance of the Al/PS/n-Si at zero bias was measured and found to be 16.4nF.

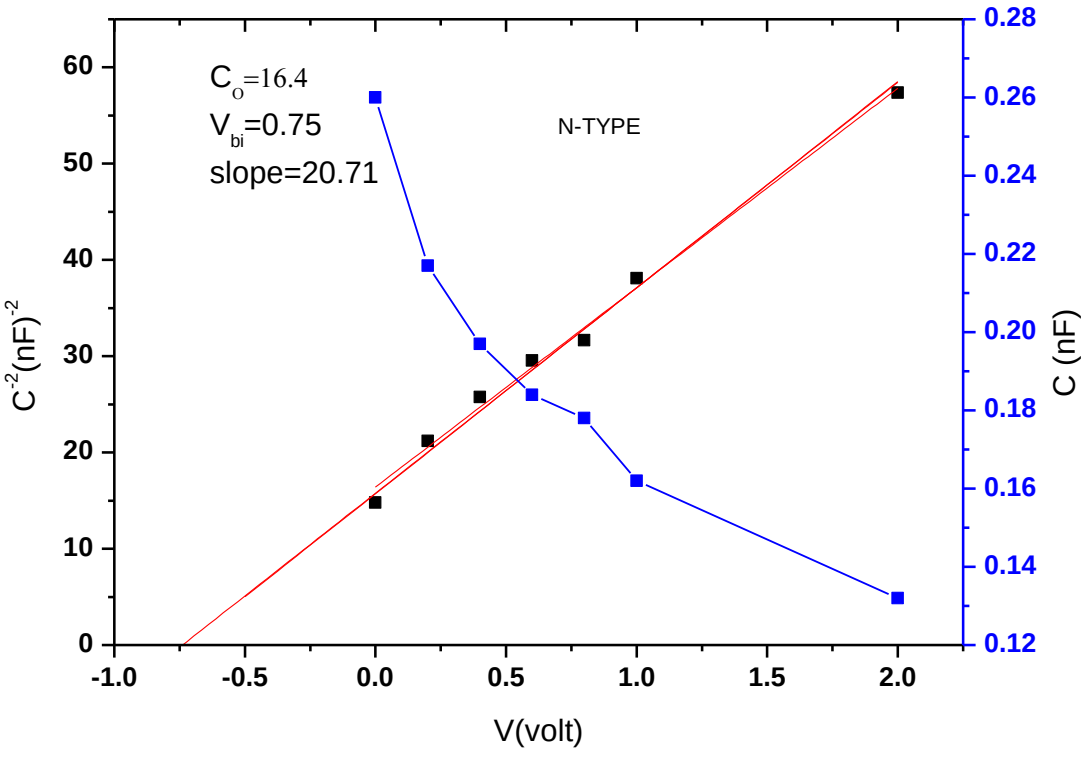

Figure 4. Capacitance-voltage and reverse bias C^2-V characteristics for Al/PS/n-Si/Al recorded at 200 KHz and room temperature

Capacitance of a Schottky diode can be represented by Eq. (3). It predicts a linear relationship between (C^2) and V under strong bias conditions. The carrier density (N_c) values used in the calculations are determined from the slope of the linear part plot of C^2 vs. V curves [12].

$$\text{slope} = \frac{2}{A^2 \epsilon\, q\, N_c} = \frac{V_{bi}}{C^2} \quad \text{..... (6)}$$

$$\emptyset_{b=} V_{bi} + \frac{KT}{q} \ln\left(\frac{N_c}{N_A}\right) \quad \text{..... (7)}$$

Fig. 5 shown the capacitance-voltage and C^2-V of the Al/PS/p-Si were measured at frequency of 200 KHz in dark at room temperature. It is clear that the capacitance decreases with increasing of the reverse bias voltage. The capacitance of the Al/PS/p-Si at zero bias was measured and found to be 1.22 nF.

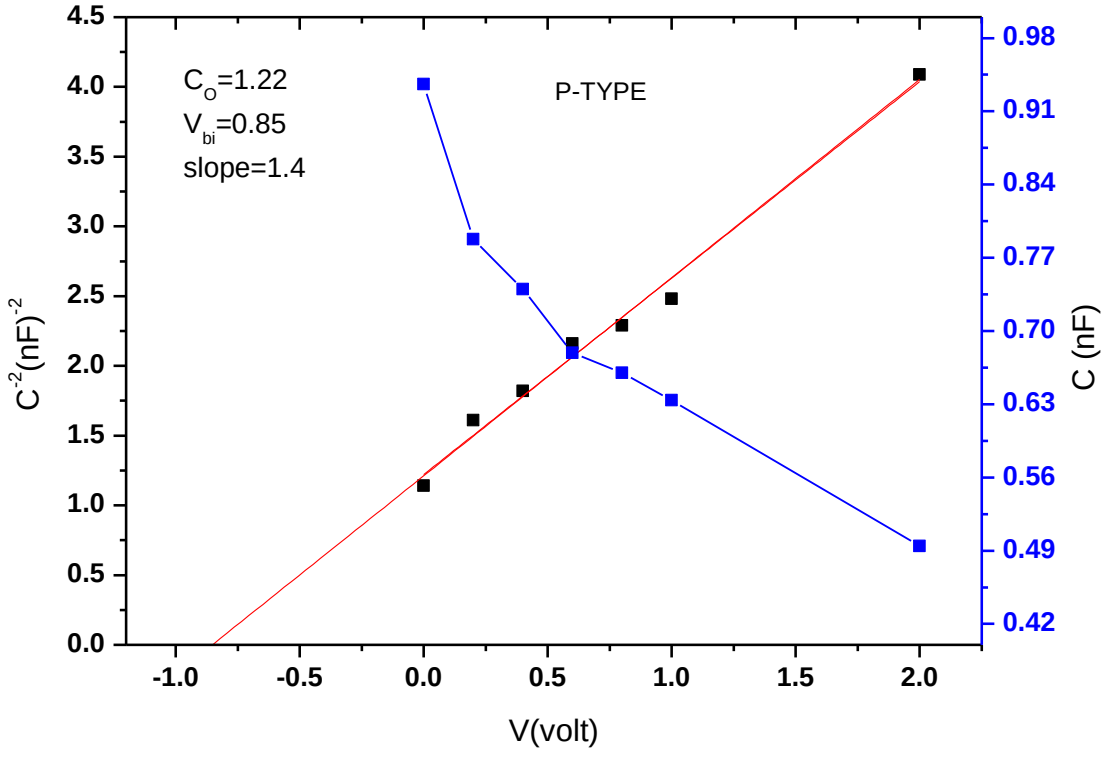

Figure 5. Capacitance-voltage and reverse bias C^2-V characteristics for Al/PS/p-Si/Al recorded at 200 KHz and room temperature

The extracted Built in voltage, N_C , N_V, N_A, N_DConcentration and Barrier height for the Al/PS/p-Si/Al and Al/PS/n-Si/Al devices are provided in Tables 4. The values of built in voltage was calculated from the x-intercept of Figures 4 & 5 and using Eq. (7) for Al/PS/n-Si and Al/PS/p-Si structures, the capacitance-voltage barrier height for Al/PS/n-Si Schottky

diode was 0.758 and 0.792 for the Al/PS/p-Si Schottky diode. Built-in potential and the calculated N_V and N_c for the tow devices are provided in Tables 4. The value of barrier height obtained from the forward bias C–V is lower than from the reverse bias I–V measurement.

Table 4. Built in voltage and Schottky barrier height of Al/PS/n-Si and Al/PS/p-Si measured from (C-V)

Wafer silicon	Doping Concentration cm^{-3}	conduction and valance concentration cm^{-3}	Built in voltage V_{bi}	Barrier height $\emptyset_b$
p-type	$N_A = 2.75 \times 10^{14}$	$N_C = 1.95 \times 10^{14}$	0.85	0.792
n-type	$N_D = 8.35 \times 10^{14}$	$N_V = 1.64 \times 10^{13}$	0.75	0.758

These results of Schottky barrier height were shown inhomogeneity at the interfaces and when the trap states exist on the metal-semiconductor boundary, the value of the barrier height does not depend only on the contact materials [15] and barrier height is likely to be a function of the interface atomic structure, and the atomic inhomogeneity at the metal-semiconductor interface which are caused by grain boundaries, multiple phases, facets and defect [5].

4. CONCLUSION

The Schottky barrier height of the contacts were deduced from the I-V and C-V characteristics and analysed by using the thermionic emission model. The rectifier factor for Al/PS/n-Si/Al Schottky diode is approximately 100 times higher as compared to that for Al/PS/p-Si/Al structure. It has been found the influence of the presence of interface porous silicon layer on the Schottky diode performance and the net effect of Schottky diode with PS layer for n-type was to lower the potential barrier at the junction compare with p-type. The states associated with the defects near surface of the semiconductor lead to the ideal factor large then one. Schottky barrier height deduced from current-voltage and capacitance-voltage were not always the same.

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