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Comparative study on transistor based full adder designs

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ABSTRACT

Recently in the generic systems the load on the processor is much heavy. The ability and the challenging process have ended with larger core operations are in the core processor. This paper is basically given special importance on different methodologies having been proposed for Adder, which is the basic operation of the Arithmetic unit. The wide research on the digital adders has been covered so many applications like designs of ALU, RISC, CISC processors, DSP used for data path arithmetic, low power CMOS, optical computing, Nanotechnology and so on. This paper gives greater knowledge and understanding about the various techniques that have amply used of Adder from the earlier years. In this paper we analyzed the implementation of different types of full Adders implemented using CMOS logic (Static CMOS and Dynamic CMOS), CMOS Transmission Gates, Pass Transistor Gates (CPL and DPL).

***Keywords*:** Full Adder; CPL; DPL; CMOS; Transmission gates; Arithmetic Unit

1. INTRODUCTION

In the ALU, the most important arithmetic is the Full Adder block. Full adder is the basic unit in almost all computational circuits. Low power techniques applied on Full Adder block can reduce the computational power consumption. Several full adder circuits have been proposed targeting on design accents such as power, delay, speed and area [1].

Digital Logic Circuit implementation can be done by using so many various designs Techniques. Recent years there are lot of literature has appeared to have the basic logic functions in the innovative digital designs. The innovative designs includes gates built using CMOS logic (Static CMOS and Dynamic CMOS), CMOS Transmission Gates, Pass Transistor Gates (CPL and DPL). In the static CMOS circuits, the pMOS and nMOS transistors are in duality principle. Transmission gate is built with a parallel connected pMOS and nMOS, where complementary input signals will be given to the gate of both the transistors. So the transmission gate will be working as a bidirectional switch. But in transmission gate we have the disadvantage of time-skew problems can lead to short circuits. So that logic can be reduced by using the CPL. It consists of pure nMOS or only pMOS transistors involved in the logic operations. But threshold voltage drop will be very high in case of using only nMOS transistor. So for low voltage applications instead of using CPL, we can use the DPL to design the logics. [2]

The implementation of full adders can have several categories. The conventional full adder uses the static CMOS and complementary Pass transistor logics (CPL). In last few decades, so many new designs have been evolved for the deep submicron technology. Based on this the review on full adder is done and presented in this paper. There are several improvements had been made in the parameters such as Area, power, delay and speed.

In this review paper we started analyzing with the conventional 28T full adder circuit using Static CMOS logic and then gradually moving towards the full adder implemented with less than 8T is summarized.

2. LITERATURE REVIEW

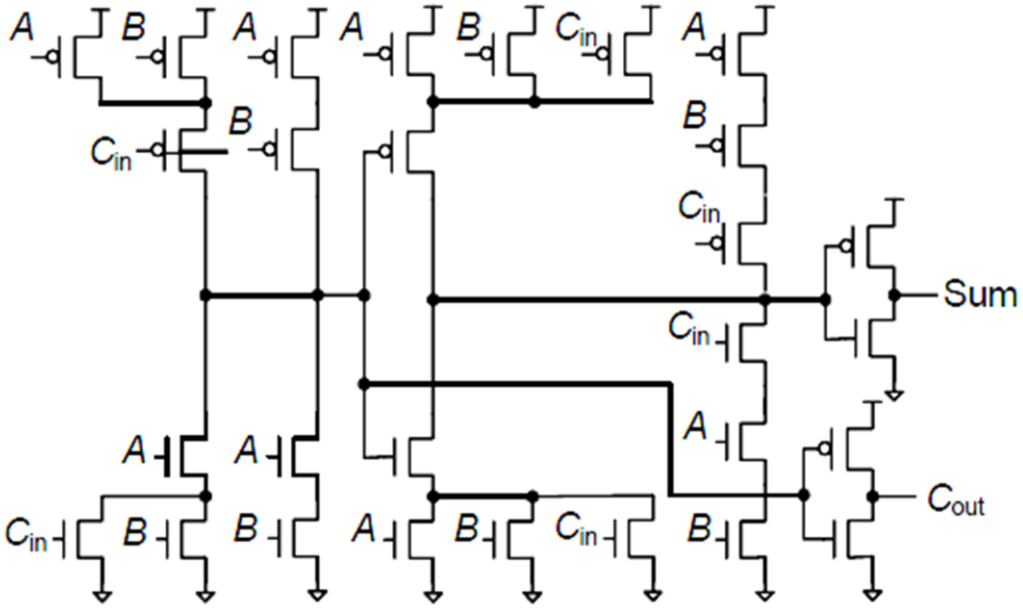

Fig. 1 – conventional 28T full adder circuit.

"In 1992, N. Zhuang and H. Wu, "A New Design of the CMOS Full Adder", IEEE Journal of Solid-State Circuits".

Full adder circuit is designed using CMOS Transmission gates with and without driving outputs. And the design is compared with the conventional Full Adder design using Static CMOS gates which has 28T shown in Fig. 1. Using the transmission gate design 4T has been reduced.

In 1997, R. Zimmermann and W. Fichtner , "Low-Power Logic Styles: CMOS Vs Pass-Transistor Logic" IEEE Journal of Solid-State Circuits

In this paper, full adder designed in complementary MOS logic is compared with pass-transistor logic as shown in Fig.1 and fig. 2. With only few exceptions Complementary CMOS, however, proves to be superior to CPL with respect to speed, area, power consumption, and power-delay products. CMOS to be 20% faster and superior to CPL, even though CPL was found to be the most efficient. An implemented 32-bit adder using complementary CMOS has a power-delay product of less than half that of the CPL version. The paper shows that complementary CMOS is the logic style of choice for the implementation of arbitrary combinational circuits, if low voltage, low power, and small power-delay products are of concern. Complementary static CMOS performs much better than CPL and other pass-transistor logic styles if low power is of concern.

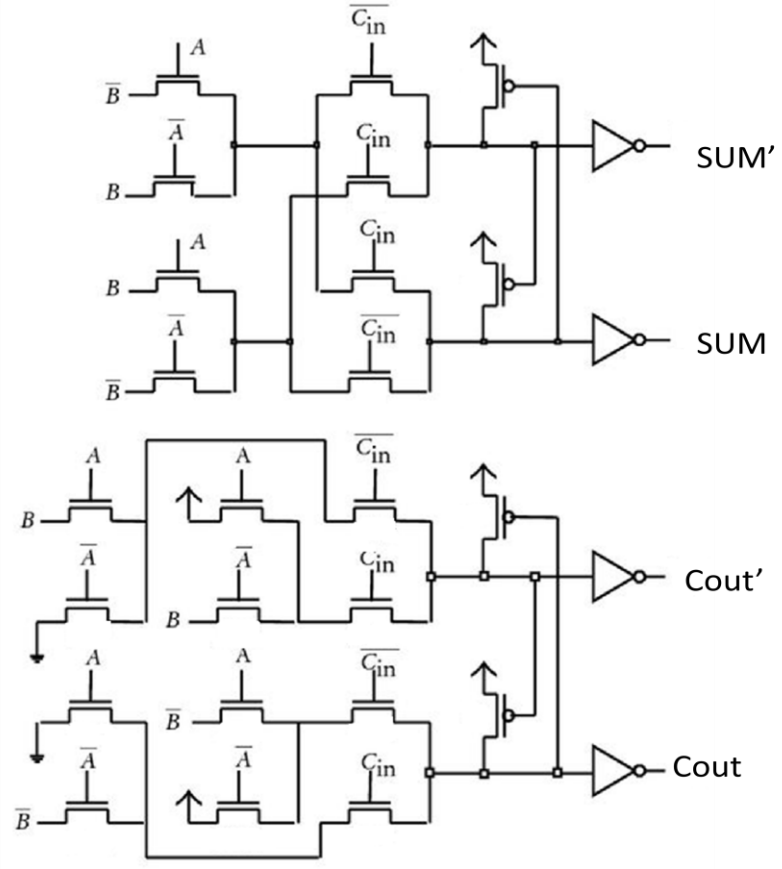

Fig. 2 Full Adder using CPL

In the year 1999, R. Shalem, E. John, and L. K. John, "A Novel Low-power Energy Recovery Full Adder Cell"

SERF – Static Energy Recovery Full Adder with 10T circuit is designed and implemented in this paper. Energy efficient circuit is based on the energy recovering logic is used. By using this logic energy consumption is very less than the non energy recovering circuit. It takes approximately 26% to 55% less energy than the other designs and is shown to be 19% faster. So SERF circuit fig. 3 is more superior than the other circuits.

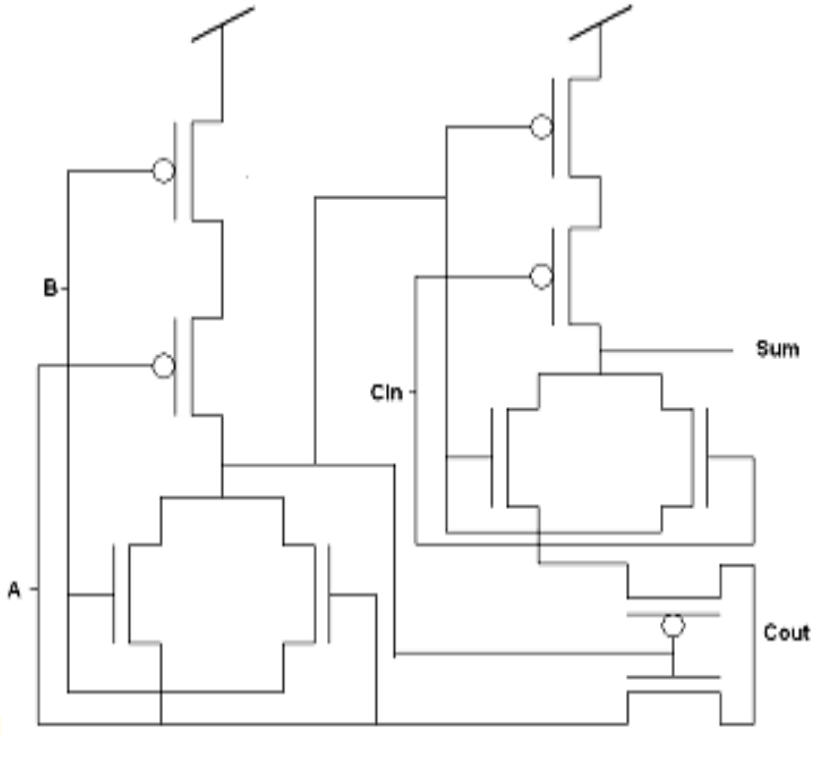

Fig. 3. SERF adder circuit with 10T

In the same year 1999, M. Vesterbacka, "Signal Processing Systems", IEEE Conference Publications"

In this paper its explained how XOR and XNOR circuits are used to realize a 1-bit full adder circuit based on transmission gates. A 6T CMOS XOR circuit that also produces a complementary XNOR output is introduced in the full adder. The resulting full adder circuit is realized using only 14T and compared with existing 16T full adder circuit [2]. Both circuits are shown in Fig.4 and fig.5 respectively. Also the layout of 14T and 16T full adder cells have been designed and simulated for comparison. Both adders yield similar performance in terms of power consumption, propagation delay and power delay product, but 14T adder cell has the advantage of full voltage swing at all circuit nodes.

The area is somewhat lower for the proposed adder on account of reduced device count. However, due to two feedback MOSFETs in the proposed adder that need to be ratioed, there is a higher cost in terms of design effort.

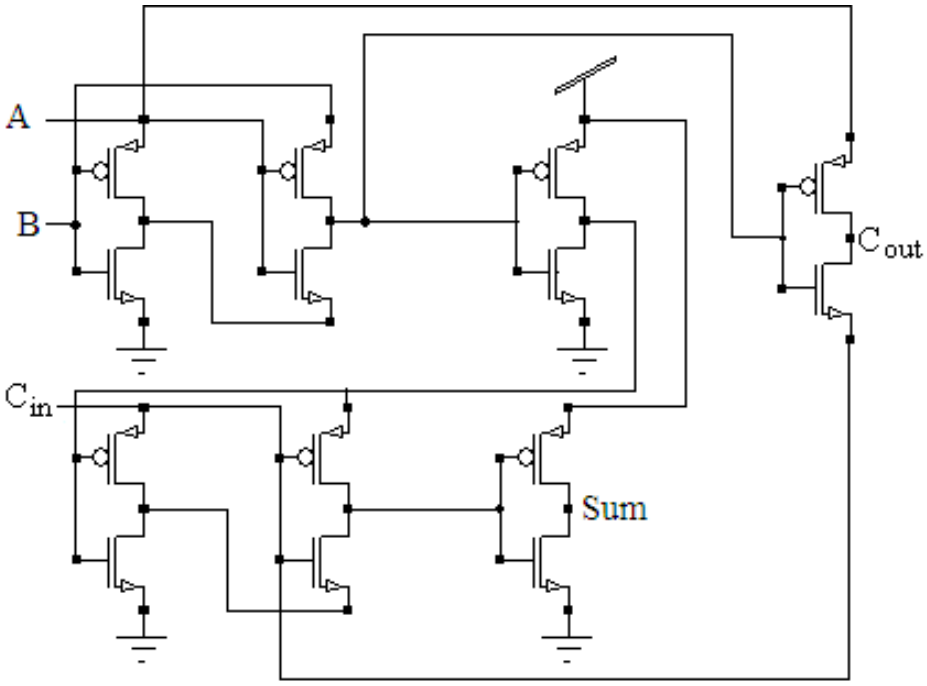

Fig. 4. 14T Full Adder.

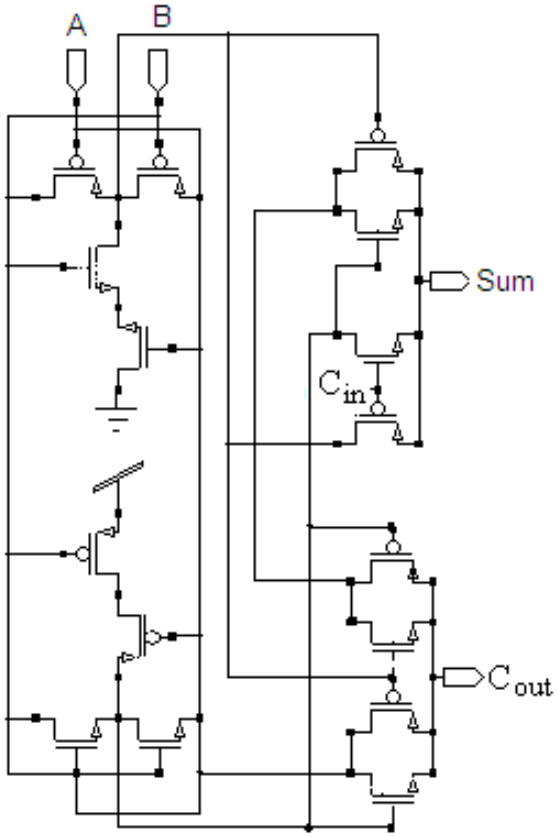

Fig. 5. 16T full adder using Transmission gates.

Further in 2001, D. Radhakrishnan, "Low-Voltage Low-Power CMOS Full Adder", IEE Proc.- Circuits Devices Systems

XOR – XNOR gate using CMOS Pass transistor logic is designed, which fully compensated the threshold voltage drop. When the power supply is scale down for certain bounds, as long as the sizing of CMOS transistor in the initial stage of design. So with less number of transistor count leads to the low power and high speed. In this paper they designed 14T, 16T and fully restored CMOS full adder with 14T and simulated in the .35µm technology.

In 2002, H.T.Bui, Y.Wang, and Y.Jiang, "Design and Analysis of Low-Power 10-transistor Full Adders using XOR-XNOR gates"

In this paper, proposed a technique along with the existing ones to build a total of 41 new 10-transistor full adders using novel XOR and XNOR gates in combination. Simulation has been carried out with different adders and different input test patterns, load capacitance and frequencies using HSPICE. When compare to the previous circuits this new adder consumes on average of 10% less power and have higher speed. One con in this circuit is the threshold-voltage loss of the pass transistors.

In 2004, Y. Jiang, A. A. Sheraidah, Y. Wang, E. Sha, and J. G.Chung, "A Novel Multiplexer based Low-Power Full Adder"

This paper constitute based on the multiplexer based Full adder, which as designed using 12T. This MUX based FA has reduced number of logic transition and low short circuit current when compare to the previous FA. They compared the 12T MUX based FA with the conventional 28T FA and four other 10T FA [4] – [7] using HSPICE. This designed has achieved 26% less power than the conventional and 23% than 10T and 64% speed is increased.

In 2005, F. Vasefi and Z. Abid, "Low Power N-bit Adders and Multiplier Using Lowest Number of Transistors 1-bit Adders"

In this they proposed two designs of 10T adder as shown in Fig. 6 and one 12T full adder by adding two extra stack transistors to 10T adder. 10T adder suffers from threshold loss while 12T eliminated this problem completely. The 10T adder achieved a 43.68% improvement in power consumption. Both proposed adders were further used to implement 4-bit RCA and 4×4 array multiplier. The schematic of 12T adder is shown in Fig. 6 (b).

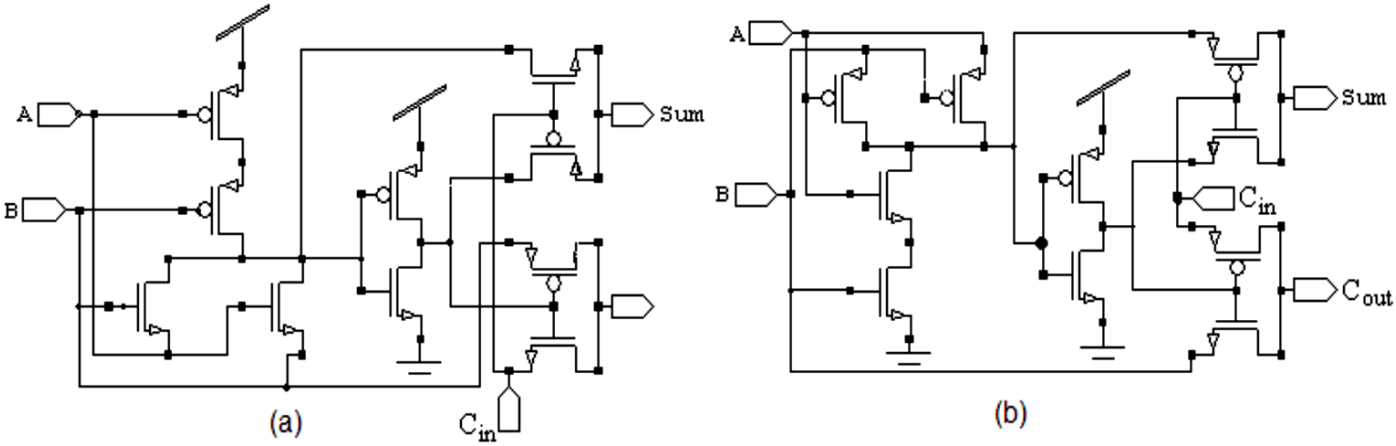

Fig. 6. 10T Full Adder

In 2006, A. Saberkari and S. B. Shokouhi, "A Novel Low-Power Low-Voltage CMOS 1-Bit Full Adder Cell with the GDI Technique"

XOR – XNOR gates has been implemented using GDI techniques and a new design is drawn for Full Adder. Even though the area is very large, it has low power – delay product and energy efficient over a wide range of voltages among all the other logics.

In 2007, P. Lee, C Hsu and H.Y. Hung, "Novel 10T Full Adders realized by GDI Structure".

Full Adder is implemented using GDI techniques with 4T GDI XOR – XNOR gates shown in fig. 7. Using this 4 different types 10T adder has been implemented and compared. The proposed designs possess the advantage of flexibility, less transistor counts and improved power consumption as well as delay making it a better alternative.

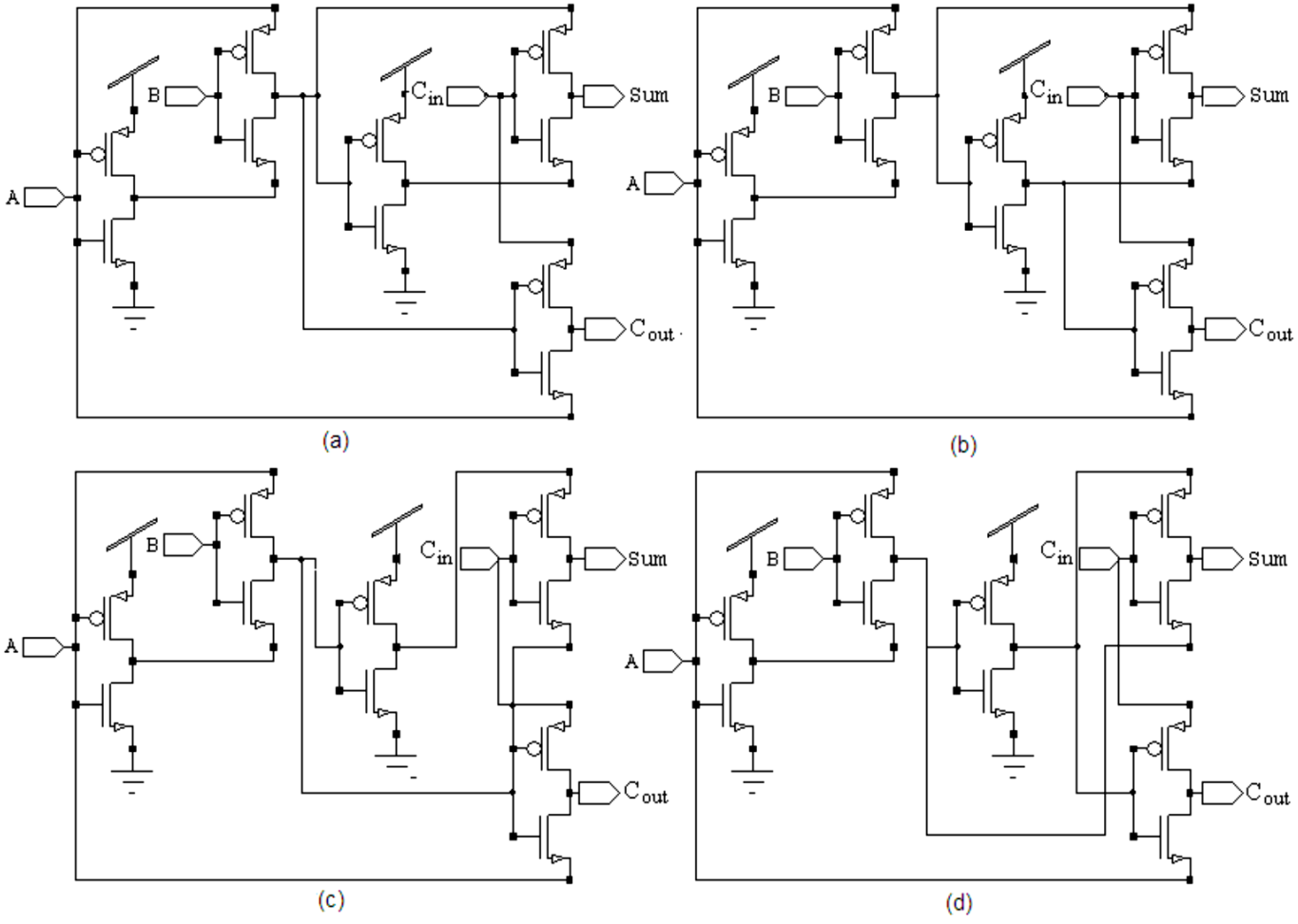

Fig. 7. 4T GDI XOR – XNOR gates

In 2008, K. Navi and O. Kavehei, "Low-Power and High-Performance 1-Bit CMOS Full- Adder Cell"

1 bit Adder is designed using bridge style and compared with conventional CMOS Adder. At room Temperature Bridge style CMOS Adder is simulated using HSPICE in 90 nm

technology, and under given conditions, an improvement of 41.5% in speed over conventional CMOS adder is achieved. In addition, the suggested adder shows 13.8 to 31.5% degradation in terms of power consumption than conventional CMOS design with different power supply. In addition, the delay and average power consumption results depict impressive improvement of 60% over conventional CMOS counterpart in power-delay product.

Entering the year 2009, M.Hosseinghadiry, H. Mohammadi and M.Nadisenejani, "Two New Low-Power High-Performance Full Adders with Minimum Gates"

XOR is designed using 3T and XNOR with 4T designed and by using this design 10T and 9T full adder is implemented and evaluated the performance with the 12T. 10T circuit shown in Fig. 7 (b) has threshold loss problem due to degraded XNOR output and output multiplexers. 9T adder shown below in Fig. 8 showed 24% improvement in term of power consumption and has better PDP for different operating voltages as well as frequencies but 10T adder is 12% faster than earlier reported full adder cells.

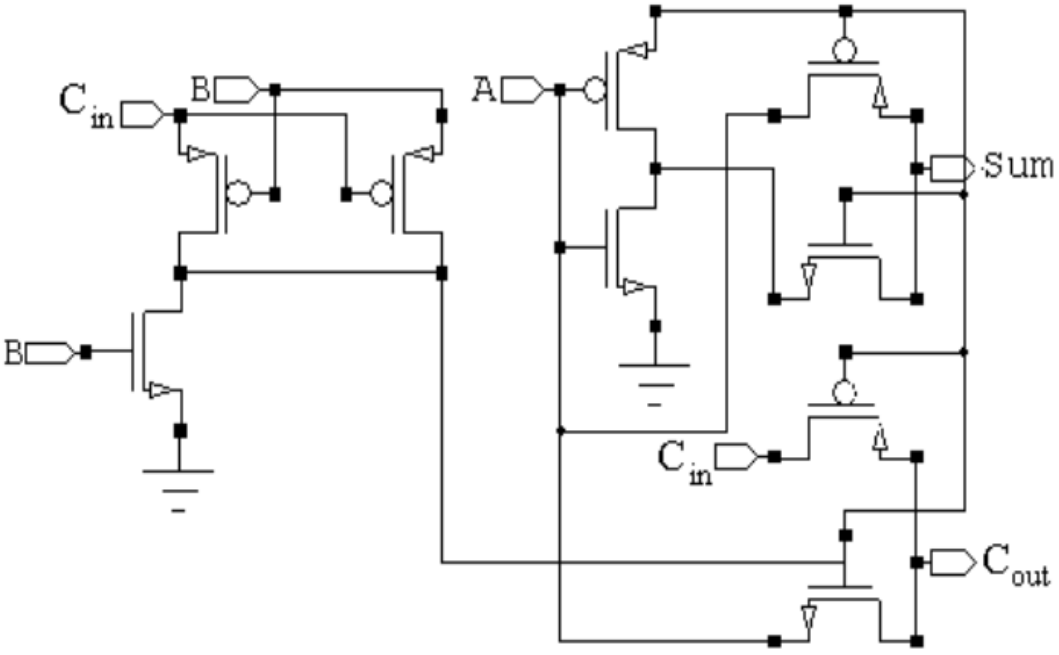

Fig. 8. 9T Full Adder

In 2010, Tripti Sharma, K.G.Sharma, Prof.B.P.Singh and Neha Arora, "A Novel CMOS 1-bit 8T Full Adder Cell"

Did the modification by changing aspect ratios of the transistors of earlier proposed 8T adder shown in Fig. 9. By reducing the transistor size the threshold loss remains the same while reducing the power consumption. This effort results into low power adder design.

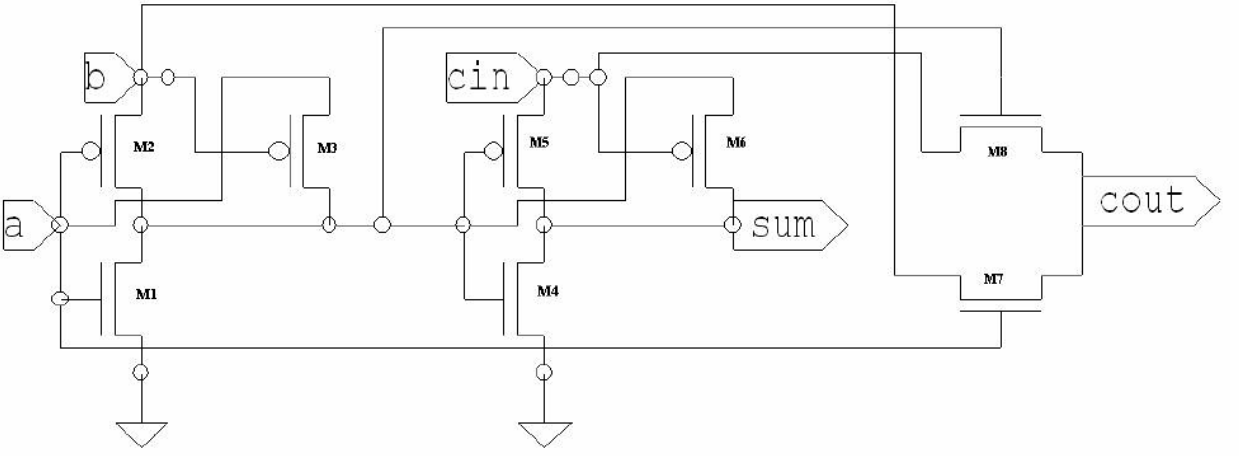

Fig. 9. 8T Full Adder [12]

Step to 2011, Shivshankar Mishra, V. Narendar and Dr. R. A. Mishra, "On the Design of High-Performance CMOS 1-Bit Full Adder Circuits

Using Cadence VIRTUOSO environment in 180 nm technology with 9 transistor and 10T Adder circuit at different supply voltages. And it was concluded that have a great signal level, less power and high speed. The designed circuit is 19% to 47% faster than the conventional Full Adder and 6% to 67% less power. Both the proposed circuit is given in the Fig. 10.

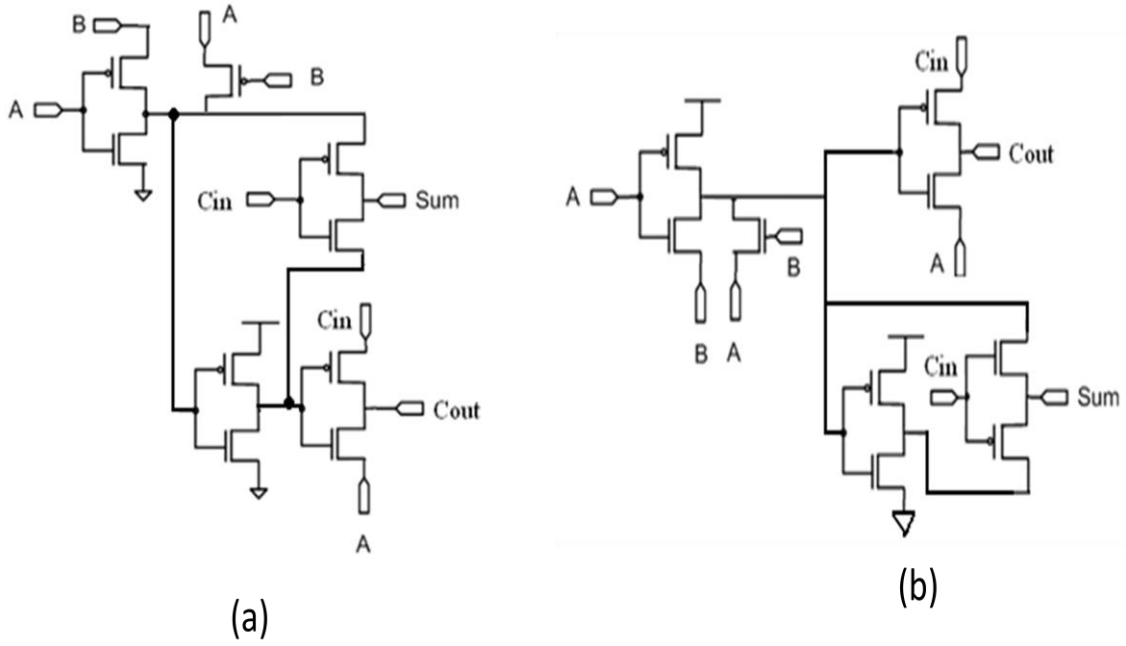

Fig. 10. 9T Full adders using XOR and XNOR cells

Further in 2011, Deepa Sinha, Tripti Sharma, K. G. Sharma and Prof. B. P. Singh " Ultra Low Power 1-Bit Full Adder"

The 8T adder due to simultaneous enabling of two transistors by adding an extra transistor and gives full voltage swing at low supply voltage. This circuit has eliminated serious threshold problem in This circuit shows improvement in power, delay and power-delay product with varying operating voltages, frequencies under different temperature ranges. The proposed circuit is shown in Fig. 11.

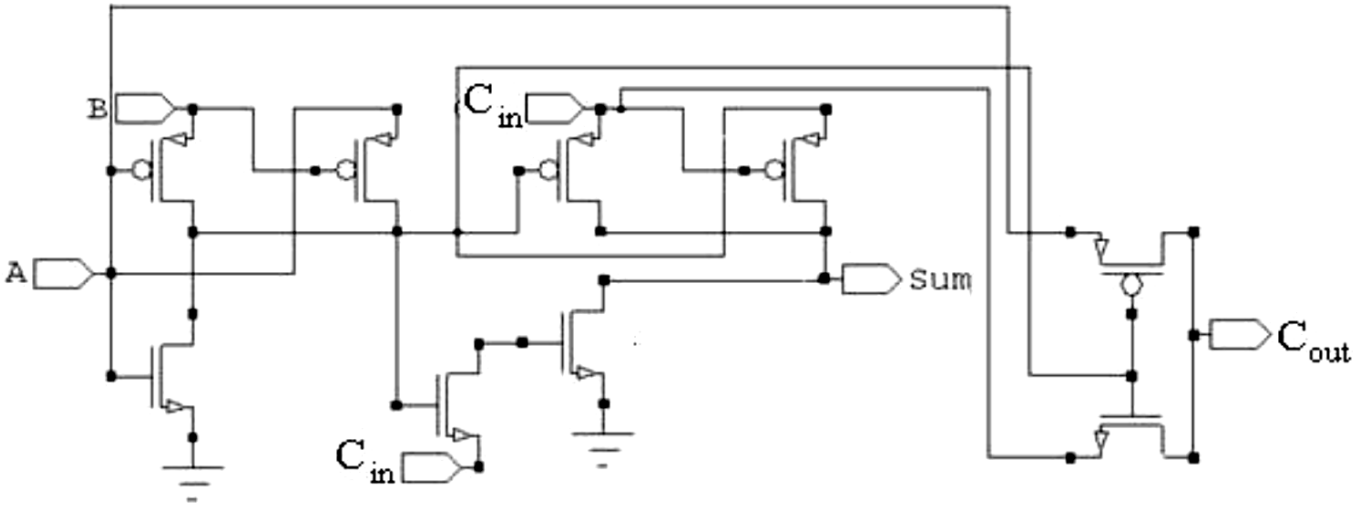

Fig. 11. 9T Full adder with extra added nMOS [14]

Then in the same year, M. Kumar, S. K. Arya and S. Pandey, "Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate"

In present work a new XNOR gate using three transistors has been presented, which shows power dissipation of 550.7272 µW in 0.35 µm technology with supply voltage of 3.3V. Minimum level for high output of 2.05V and maximum level for low output of 0.084V have been obtained. A single bit full adder using eight transistors has been designed using proposed XNOR cell, which shows power dissipation of 581.542 µW.

Minimum level for high output of 1.97V and maximum level for low output of 0.24V is obtained for sum output signal. For carry signal maximum level for low output of 0.32V and minimum level for high output of 3.2V have been achieved.

Power consumption of proposed XNOR gate and full adder has been compared with earlier reported circuits and proposed circuit's shows better performance in terms of power consumption and transistor count. The proposed Full adder with XNOR and MUX is shown in Fig. 12.

In 2012, A. Bazzazi, A. Mahini and J. Jelini, "Low Power Full Adder Using 8T Structure"

In this paper 8T adder circuit is implemented with sizing of the transistors. FA operates in 100 MHz range. The 5% variation of power supply and also several temperatures are measured. In this paper author has changed the substrate biasing of CMOS and also compatible with transistor size 10% variation. The power consumption of this adder is 200nw.

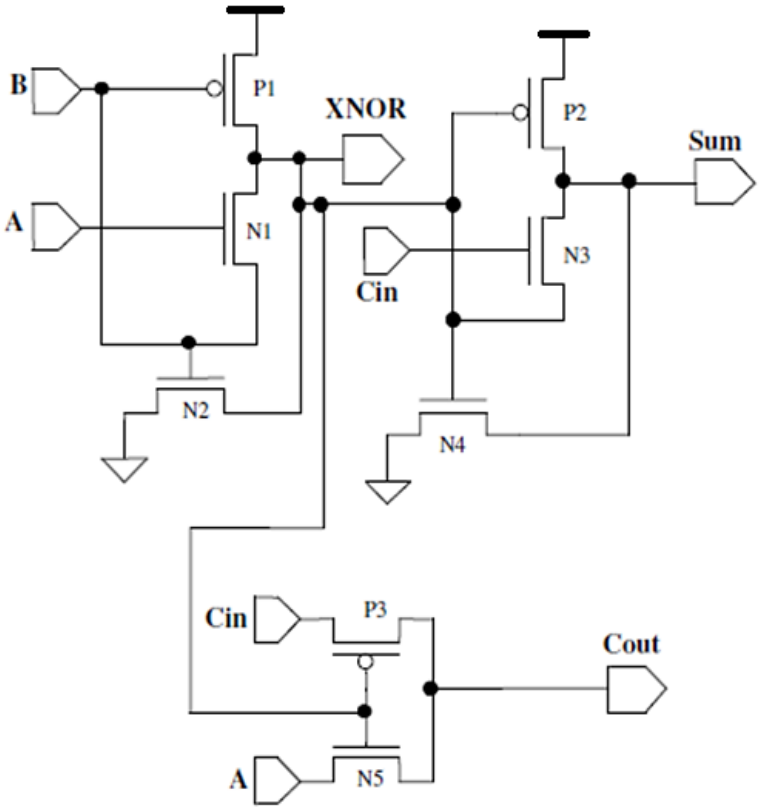

Fig. 12. Full adder using two XNOR gates and multiplexer

In 2013, M.Geetha Priya, K.Baskaran," Low Power Full Adder With Reduced Transistor Count"

This paper presents the 3T XOR gate with sufficient area and power. New 8T full adder is designed using this 3T XOR gate since conventional Full adder circuit increases the overall computational delay. Low power consumption and high speed has achieved when it was simulated in 90 nm CMOS technology using HSPICE at room temperature. 89% average power consumption has improved in this method.

The simulation result is shown in the given Table. 1.

Table 1. Simulation results for the proposed full adder circuits in 90nm Process technology at 50 MHz frequency.

Adder	No. of Transistors	Power (nW)	Delay (ps)	PDP (E^{-21} J)
CMOS	28	54.72	375.2	20530
CPL	32	76.82	462.8	35552
TGA	20	42.99	282.5	12144

TFA	16	41.02	297.1	12187
HPSC	22	38.83	539.8	20960
Hybrid CMOS	24	34.68	372.9	12932
14T	14	45.29	427.6	19366
Proposed 8T	8	5.87	288.4	1692

3. CONCLUSION

Concisely, the above discussion on literature reveals that all the modifications and size shrinking of single bit full adders are done to improve the power consumption of the cell so that it can be better useful for portable applications. The delay got reduced for a certain designs and the speed of the full adder circuit is increased. So the arithmetic unit of the processor will give the result very faster as the technology develops.

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